8V to 40V Low Standby Current Pulse Width Modulator (PWM) Control Circuit

Features

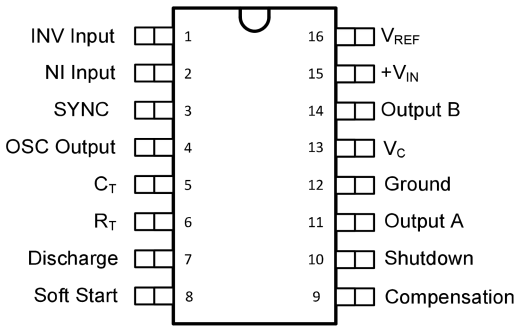
- 8-V to 40-V Operation
- Low Standby Current: 5.0 mA
- 5.1-V Reference Trimmed to 1%
- 100-Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Dead-Time Control
- Internal Soft Start
- Pulse-by-Pulse Shutdown
- Input Under-voltage Lockout With Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source and Sink Output Drivers
- Available Packaging: SOP16/WSOP16/TSSOP16/DIP16

Applications

- Solar Inverters
- Welding Inverters
- Motor Control
- Battery Chargers
- DC/DC Power Supplies
- Converters Using Voltage Mode

General Description

The COSG3525A/3527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip 5.1-V reference is trimmed to 1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between CT and the discharge terminals provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands.



Pin Diagram

Rev1.1

1. Pin Configuration and Block Diagram

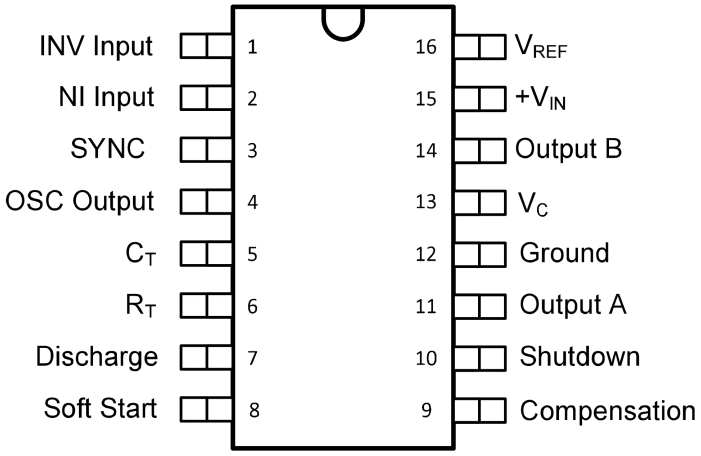


Figure 1 Pin Diagram (SOP16/WSOP16/TSSOP16/DIP16)

Pin Description

Pin	Name	I/O	Description
1	INV Input	I	Inverting input to the error amplifier
2	NI Input	I	Non-Inverting input to the error amplifier
3	SYNC	I	Oscillator sync terminal
4	OSC Output	O	Oscillator output
5	C_T	I	Timing capacitor connection pin for oscillator frequency programming. It should be connected to the device ground using minimal trance length.
6	R_T	I	Timing resistor connection pin for oscillator frequency programming
7	Discharge	I	A single resistor between C_T and the discharge terminals provides dead-time adjustment.
8	Soft Start	I	Soft-start input pin
9	Compensation	O	Output of the error amplifier for compensation
10	Shutdown	I	Pull this pin high to shut down PWM output
11	Output A	O	Output A of the on-chip drive stage
12	Ground	P	Ground return pin
13	V_C	P	Power supply pin for the output stage. This pin should be bypassed with a 0.1-μF ceramic low ESL capacitor with minimal trace lengths.
14	Output B	O	Output B of the on-chip drive stage
15	$+V_{IN}$	P	Supply voltage
16	V_{REF}	O	5.1V reference. For stability, the reference should be bypassed with a 0.1-μF ceramic low ESL capacitor and minimal trace length to the ground plane.

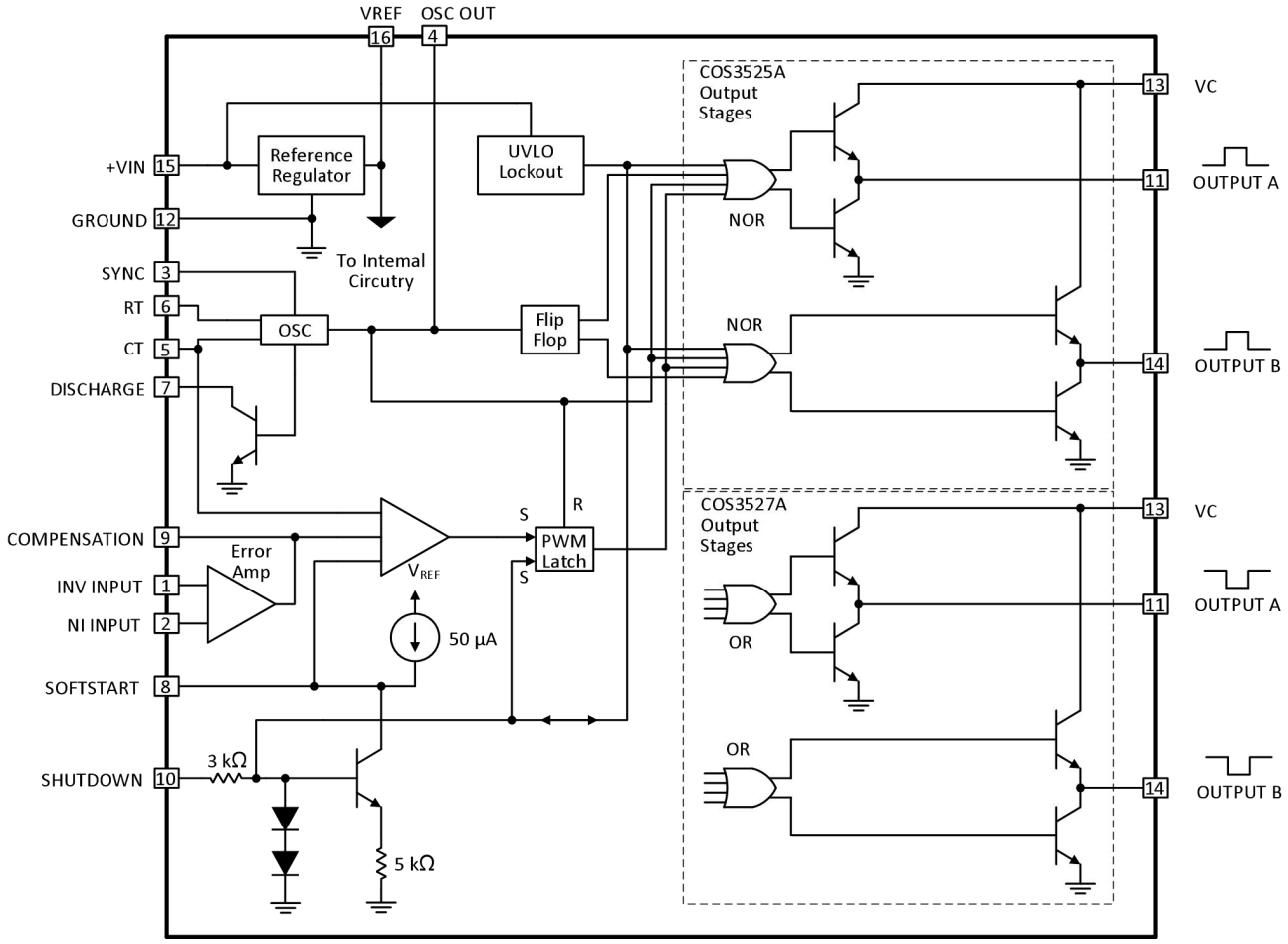


Figure 2. Block Diagram

2. Ordering Information

Model	Order Number	Package	Package Option	Marking Information
COSG3525A	COSG3525AP	SOP-16	Tape and Reel, 3000	COSG3525AP
	COSG3525AT	TSSOP-16	Tape and Reel, 3000	COSG3525AT
	COSG3525ADWR2G	WSOP-16	Tape and Reel, 1500	COSG3525ADW
	COSG3525AN	DIP-16	Tube, 50	COSG3525AN
COSG3527A	COSG3527AP	SOP-16	Tape and Reel, 1500	COSG3527AP
	COSG3527AT	TSSOP-16	Tape and Reel, 3000	COSG3527AT
	COSG3527ADW	WSOP-16	Tape and Reel, 1500	COSG3527ADW
	COSG3527AN	DIP-16	Tube, 50	COSG3527AN

3. Product Specification

3.1 Absolute Maximum Ratings (1)

Parameter	Min	Max	Unit
Supply Voltage $+V_{IN}$		41	V
Collector Supply Voltage V_C		41	V
Logic Inputs	-0.3	5.5	V
Analog Inputs	-0.3	$+V_{IN}$	V
Output Current, Source or Sink		500	mA
Reference Output Current		50	mA
Oscillator Charging Current		5	mA
Operating Junction Temperature	-40	+125	°C
Storage Temperature	-55	+150	°C

(1) Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

3.2 Thermal Data

Parameter	Rating	Unit
Package Thermal Resistance	80 (SOP16) 110 (TSSOP16) 70 (DIP16)	°C/W

3.3 Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage $+V_{IN}$	8	-	40	V
Collector Supply Voltage V_C	4.5	-	40	V
Sink/Source Load Current (Steady State)	0	-	100	mA
Sink/Source Load Current (Peak)	0	-	400	mA
Reference Load Current	0	-	20	mA
Oscillator Frequency Range	0.1	-	500	kHz

Oscillator Timing Resistor	2	-	150	kΩ
Oscillator Timing Capacitor	0.001	-	0.01	μF
Dead Time Resistor Range	0	-	500	Ω
Operating Junction Temperature	-40	-	+125	°C

3.4 Electrical Characteristics

(Typical values are tested at V_{IN}=20V, T_A=25 °C, unless otherwise specified.)

Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY						
Supply Voltage	V_{IN}		8	-	40	V
Total Standby Current	I_S	V_{IN} = 20 V	-	5	7	mA
REFERENCE						
Output Voltage	V_{REF}		5.0	5.1	5.2	V
Line Regulation	ΔV_{REF}	V_{IN} = 8 V to 35 V	-	10	20	mV
Load Regulation	ΔV_{REF}	I_L = 0 to 20 mA	-	20	50	mV
Temp. Stability	ΔV_{REF}	Over operating range		20	50	mV
Total Output Variation	V_{REF}	Line, Load, and Temperature	4.95	-	5.25	V
Short Circuit Output Current	I_{SC}	V_{REF}=0	-	80	100	mA
OSCILLATOR						
Minimum Frequency	f_{MIN}	R_T = 200 kΩ, C_T = 0.1 μF		60	120	Hz
Maximum Frequency	f_{MAX}	R_T = 2 kΩ, C_T = 470 pF	400	430	-	kHz
Initial Accuracy	Δf		-	±2	±6	%
Voltage Stability	$\Delta f/\Delta V_{IN}$	V_{IN} = 8 V to 35 V	-	±1	±2	%
Current Mirror	I_M	I_{RT} = 2mA	1.7	2	2.2	mA
Clock Amplitude	V_{CLK}		3	4	-	V
Clock Width	$T_{W(CLK)}$		0.3	0.5	1	μs

Sync Threshold	$V_{TH(SYNC)}$		1.2	2	2.8	V
Sync Input Current	$I_{I(SYNC)}$	Sync=3.5V	-	1	2.5	mA
ERROR AMPLIFIER						
Input Offset Voltage	V_{OS}			2	10	mV
Input Bias Current	I_B		-	1	10	μA
Input Offset Current	I_{OS}		-	-	1	μA
Open Loop Voltage Gain	G_{VO}	R_L ≥ 10 MΩ	60	80	-	dB
Gain-Bandwidth Product	GBP	A_V = 0 dB	1	2	-	MHz
Common Mode Rejection Ratio	CMRR	V_{CM} = 1.5V to 5.2V	60	90	-	dB
Power Supply Rejection Ratio	PSRR	V_{IN}= 8V to 35V	50	60	-	dB
Low-level Output Voltage	V_{OL}			0.2	0.5	V
High-level Output Voltage	V_{OH}		3.8	5.6		V
PWM COMPARATOR						
Minimum Duty Cycle	$D_{(MIN)}$		-	-	0	%
Maxmum Duty Cycle	$D_{(MAX)}$		45	49	-	%
Input Threshold Voltage	V_{TH1}	Zero Duty Cycle	0.7	0.9	-	V
	V_{TH2}	Maximum Duty Cycle	-	3.3	3.6	V
Input Bias Current	$I_{B(COMP)}$		-	0.05	1	μA
SOFT START						
Soft Start Current	I_{SOFT}	V_{SD}=0V, V_{SOFT}=0V	25	50	80	μA
Soft Start Low Level Voltage	V_{SL}	V_{SD}=2.5V	-	0.3	0.7	V
SHUTDOWN						
Shutdown Threshold Voltage	$V_{TH(SD)}$	V_{SOFT}=5.1V	0.6	0.8	1	V

Shutdown Input Current	$I_{N(SD)}$	V_{SD}=2.5V	-	0.3	1	mA
Shutdown Delay	$T_{D(SD)}$	V_{SD}=2.5V	-	0.2	0.5	μS
OUTPUT DRIVERS (each output, V_C=20V)						
Low-level Output Voltage	$V_{DOL\ I}$	I_{SINK} = 20 mA	-	0.2	0.4	V
	$V_{DOL\ II}$	I_{SINK} = 100 mA	-	1	2	V
High-level Output Voltage	$V_{DOH\ I}$	I_{SOURCE} = 20 mA	18	19	-	V
	$V_{DOH\ II}$	I_{SOURCE} = 100 mA	17	18	-	V
Under-voltage Lockout	V_{UV}	V8 and V9 = High	6	7	8	V
Collector Leakage Current	I_{LKG}	V_{IN}=35V	-	-	200	μA
Rise Time	t_R	C_L=1nF	-	80	600	ns
Fall Time	t_F	C_L=1nF	-	70	300	ns

4. Functional Description

4.0 Overview

The COSG3525A/3527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The COSG3525A output stage features NOR logic, giving a LOW output for an OFF state. The COSG3527A uses OR logic, which results in a HIGH output level when OFF.

4.1 Reference

The on-chip 5.1-V reference is trimmed to 1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors.

4.2 Synchronized Input

A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock.

4.3 Adjustable Switching Frequency and Dead-Time Control

A single resistor R_D between C_T and the discharge terminals provides a wide range of dead-time adjustment. Generally, higher switching frequency gives smaller size but have higher switching loss. The switching frequency is determined by following equation:

$$f = \frac{1}{C_T(0.7R_T + 3R_D)}$$

For example, operation at 100 kHz was selected as a reasonable compromise between size and efficiency. The value of R_T = 10 kΩ, C_T = 1.37 nF and R_D = 100 Ω were chosen for 100-kHz oscillator frequency based on the equation.

4.4 Soft Start

These devices also feature built-in soft-start circuitry with only an external timing capacitor required. Soft start is achieved by connecting the soft-start pin to ground through a capacitor, charged by the 50uA current source.

4.5 Input Undervoltage Lockout with Hysteresis

The undervoltage lockout keeps the outputs off and the soft-start capacitor discharged for subnormal input voltage. This lockout circuitry includes approximately 500mv of hysteresis for jitter-free operation.

4.6 Shutdown Options

A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. Since both the compensation and soft-start terminals have current source pullups, either can readily accept a pull-down signal which only has to sink a maximum of 100uA to turn off the outputs. This is subject to the added requirement of of discharging whatever external capacitance may be attached to these pins. The shutdown pin should not be left floating as noise pickup could conceivably interrupt normal operation. All transitions of the voltage on the shutdown pin should be within the time frame of one clock cycle and not repeated at a frequency higher than 10 clock cycles.

4.7 PWM Latch

Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse.

4.8 Output Stages

The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The COS525A output stage features NOR logic, giving a LOW output for an OFF state. The COSG3527A uses OR logic, which results in a HIGH output level when OFF.

5. Typical Application Diagram

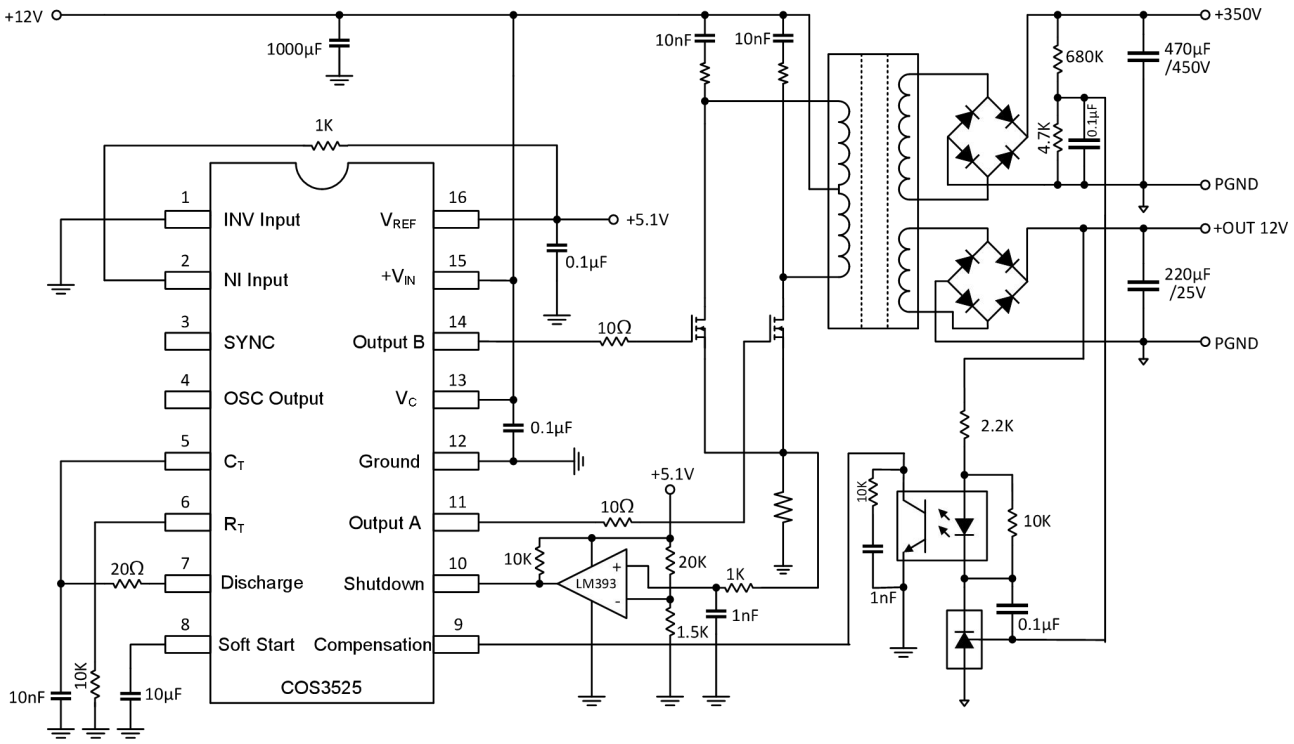
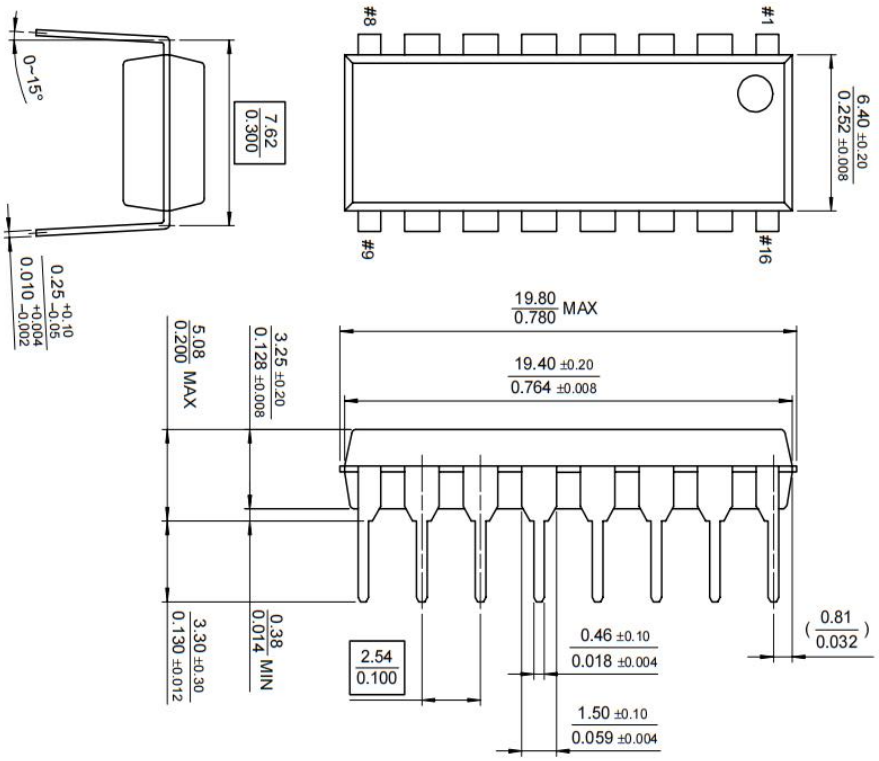


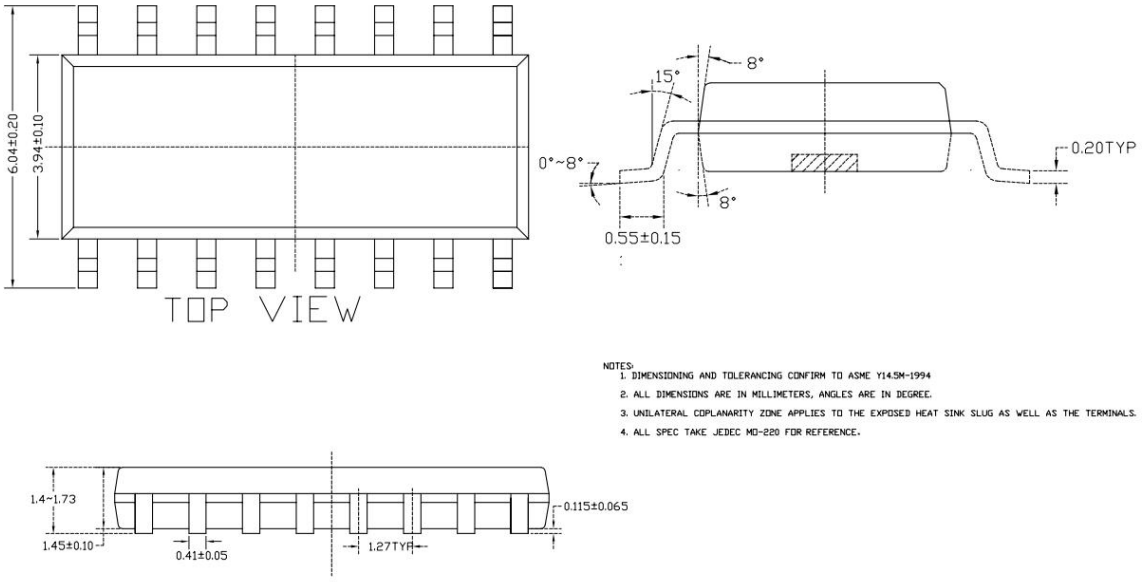
Figure 3. Typical Application in an Micro-Inverter

6. Package Information

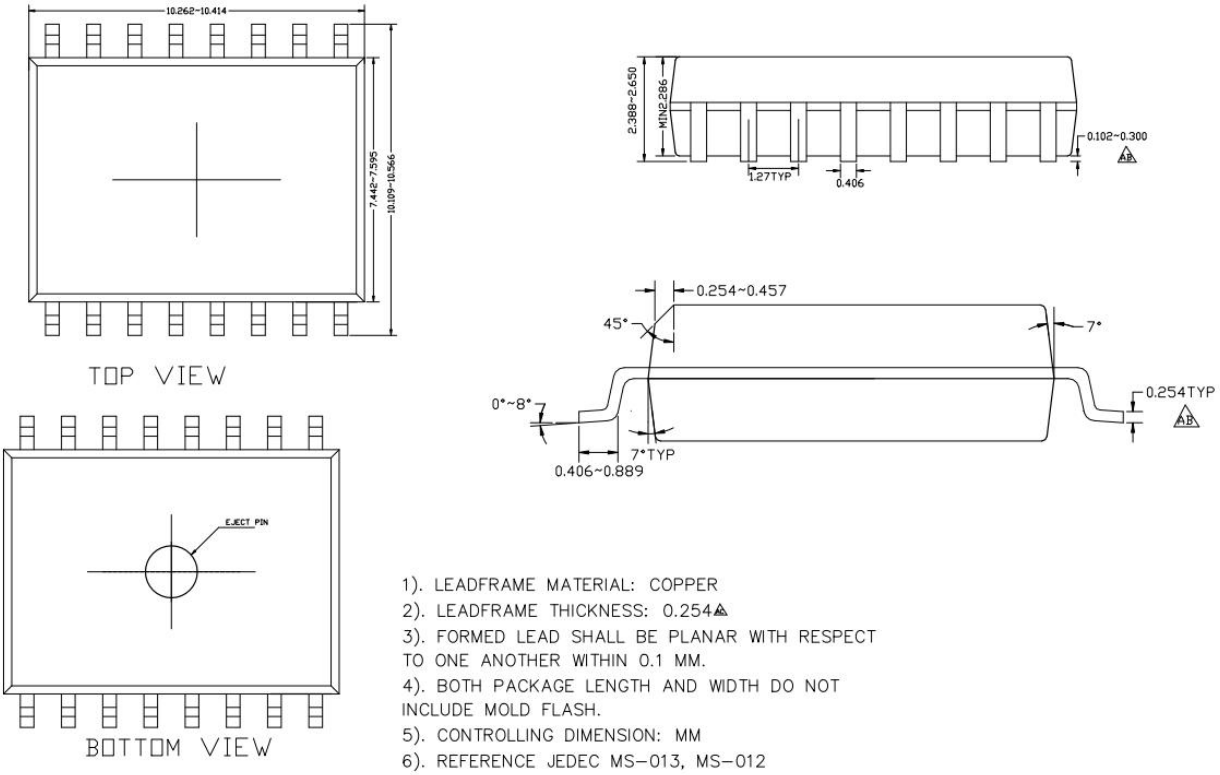
6.1 DIP16 (Package Outline Dimensions)



6.2 SOP16 (Package Outline Dimensions)



6.3 WSOP16 (Package Outline Dimensions)



1). LEADFRAME MATERIAL: COPPER
2). LEADFRAME THICKNESS: 0.254
3). FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.1 MM.
4). BOTH PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH.
5). CONTROLLING DIMENSION: MM
6). REFERENCE JEDEC MS-013, MS-012
7). THE SIZE LABEL OF THE LENGTH AND WIDTH IN THE DRAWING BELONG TO THE BOTTOM SIZE OF THE PACKAGE.